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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/617,506	07/11/2003	Shuichi Takayama	52478-4036	3981

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EXAMINER	
GEIB, BENJAMIN P	

ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 02/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/617,506	TAKAYAMA ET AL.	
	Examiner	Art Unit	
	Benjamin P. Geib	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 July 2003 and 08 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *29-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *29-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *07/11/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 29-40 have been examined.

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Application on 07/11/2003, Preliminary Amendment on 08/08/2003, Change of Address on 07/08/2005.

Priority

3. Acknowledgment is made of applicant's claim for foreign priority based on an application filed in Japan on 08/29//1997. It is noted, however, that applicant has not filed a certified copy of the 9-234354 application as required by 35 U.S.C. 119(b).

4. Acknowledgment is made of applicant's claim for foreign priority based on an application filed in Japan on 04/08//1998. It is noted, however, that applicant has not filed a certified copy of the 10-95645 application as required by 35 U.S.C. 119(b).

Specification

5. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The

disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

The abstract is lengthier than 150 words and should be amended to be within the abovementioned range of 50-150 words.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 29-38 are rejected under 35 U.S.C. 102(e) as being anticipated by Agarwal, U.S. Patent No. 5,770,894.

8. Referring to claim 29, Agarwal has taught a processor for executing an instruction sequence generated by converting a program that is capable of being described by mutually exclusive first *(conditional arithmetic instruction)* and second conditional *(conditional branch instruction capable of being replaced by a conditional arithmetic instruction)* instructions, so that the instruction sequence includes only the first conditional instruction out of the first and second conditional instructions *(See column 1, line 56 – column 2, line 2)*, wherein the processor has only the first conditional instruction out of the first and second conditional instructions *[A second*

instruction (i.e. a conditional branch instruction capable of being replaced by a conditional arithmetic instruction) is replaced with a first instruction (i.e. conditional arithmetic instruction). Therefore, the processor has (i.e. executes) only the first conditional instruction; See column 1, line 56 – column 2, line 2].

9. Referring to claim 30, Agarwal has taught the processor of claim 29, wherein the first conditional instruction is a conditional transfer instruction *(select instruction; See column 3, line 40 – column 4, line 33)*.

10. Referring to claim 31, Agarwal has taught the processor of claim 29, wherein the first conditional instruction is a conditional arithmetic instruction *(See column 4, line 36 – column 5, line 15)*.

11. Referring to claim 32, Agarwal has taught a processor for executing an instruction sequence generated by converting a program that is capable of being described by mutually exclusive first *(conditional arithmetic instruction)* and second *(conditional branch instruction capable of being replaced by a conditional arithmetic instruction)* conditional instructions, so that the instruction sequence includes only the first conditional instruction out of the first and second conditional instructions *(See column 1, line 56 – column 2, line 2)*, wherein the processor is operable to decode only the first conditional instruction out of the first and second conditional instructions *[A second instruction (i.e. a conditional branch instruction capable of being replaced by a conditional arithmetic instruction) is replaced with a first instruction (i.e. conditional arithmetic instruction). Therefore, the processor decodes only the first conditional instruction; See column 1, line 56 – column 2, line 2].*

12. Referring to claim 33, given the similarities between claim 30 and claim 33 the arguments as stated for the rejection of claim 30 also apply to claim 33.

13. Referring to claim 34, given the similarities between claim 31 and claim 34 the arguments as stated for the rejection of claim 31 also apply to claim 34.

14. Referring to claim 35, Agarwal has taught a processor for executing an instruction sequence generated by converting a program that is capable of being described by mutually exclusive first *(conditional arithmetic instruction)* and second *(conditional branch instruction capable of being replaced by a conditional arithmetic instruction)* conditional instructions, so that the instruction sequence includes only the first conditional instruction out of the first and second conditional instructions *(See column 1, line 56 – column 2, line 2)*, wherein the processor is operable to execute only the first conditional instruction out of the first and second conditional instructions *[A second instruction (i.e. a conditional branch instruction capable of being replaced by a conditional arithmetic instruction) is replaced with a first instruction (i.e. conditional arithmetic instruction). Therefore, the processor executes only the first conditional instruction; See column 1, line 56 – column 2, line 2].*

15. Referring to claim 36, given the similarities between claim 30 and claim 36 the arguments as stated for the rejection of claim 30 also apply to claim 36.

16. Referring to claim 37, given the similarities between claim 31 and claim 37 the arguments as stated for the rejection of claim 31 also apply to claim 37.

17. Referring to claim 38, Agarwal has taught a processor that executes an instruction sequence, comprising: a decoding unit operable to decode an instruction

sequence *(See column 12, lines 39-42)* generated by converting a program that is capable of being described by mutually exclusive first *(conditional arithmetic instruction)* and second *(conditional branch instruction capable of being replaced by a conditional arithmetic instruction)* conditionally instructions, so that the instruction sequence includes only the first conditional instruction out of the first and second conditional instructions *(See column 1, line 56 – column 2, line 2)*; and an executing unit operable to execute the instruction sequence decoded by the decoding unit *(See Fig. 3 and column 5, lines 5-15)*; wherein the decoding unit is operable to decode only the first conditional instruction out of the first and second conditional instructions *[A second instruction (i.e. a conditional branch instruction capable of being replaced by a conditional arithmetic instruction) is replaced with a first instruction (i.e. conditional arithmetic instruction). Therefore, the decode unit of the processor decodes only the first conditional instruction; See column 1, line 56 – column 2, line 2].*

18. Claims 39 and 40 are rejected under 35 U.S.C. 102(e) as being anticipated by Ireton, U.S. Patent No. 5,826,089.

19. Referring to claim 39, Ireton has taught an instruction conversion apparatus *(Instruction Translation Unit; Fig. 2, component 14)* for converting a program that is capable of being described by mutually exclusive first and second conditional instructions *(It is inherent that all programs are capable of being described by mutually exclusive first and second conditional instructions since all programs either a) have two*

mutually exclusive conditional instructions for their functionality or b) can be described using two additional mutually exclusive conditional operations) into an instruction sequence executable by a processor *(The instruction translation unit converts instructions from a source instruction set to a target instruction set executable by a processor; column 2, lines 34-50)*, wherein the instruction conversion apparatus, when only the first conditional instruction out of the first and second conditional instructions is decodable by the processor, interchanges

(a) a condition of the second conditional instruction with a condition of the first conditional instruction *(The instruction translation unit interchanges the condition of a second conditional instruction (i.e. a conditional instruction in the source instruction set) with a condition of a first conditional instruction (i.e. a conditional instruction in the target instruction set) by interchanging a first and second conditional instructions in the instruction stream; column 2, lines 34-50)*, and

(b) an instruction executed when the condition of the second conditional instruction is satisfied with an instruction executed when the condition of the second conditional instruction is not satisfied *(The second conditional instruction (i.e. a instruction executed when the condition of the second conditional instruction is satisfied) with the first conditional instruction (i.e. an instruction executed when the condition of the second conditional instruction is not satisfied); column 2, lines 34-50)*.

20. Referring to claim 40, Ireton has taught an instruction conversion apparatus, comprising:

an intermediate code generating unit *(Instruction Atomizing Unit; Fig. 2, component 30)* operable to generate an intermediate code sequence by converting a program *(column 5, line 52 – column 6, line 3)* that is capable of being described by mutually exclusive first and second conditional instructions *(It is inherent that all programs are capable of being described by mutually exclusive first and second conditional instructions since all programs either a) have two mutually exclusive conditional instructions for their functionality or b) can be described using two additional mutually exclusive conditional operations)*;

a detecting unit *(Dependency Checking Unit; Fig. 2, component 32)* operable to detect, from the intermediate code sequence *(column 6, lines 4-16)*,

(a) a conditional instruction *(branch instruction)* that judges whether to execute one of a first operation and a second operation

(b) a first operation code *(operation code of an instruction on the taken path of the branch)* that executes an instruction when the judgment result of the conditional instruction is to execute the first operation, and

(c) a second operation code *(operation code of an instruction on the fall through path of the branch)* that executes an instruction when the judgment result of the conditional instruction is to execute the second operation *[The dependency checking unit detects operations from the instruction atomizing unit (column 6, lines 4-6), which includes branch instructions (column 7, lines 60-68). Branch instructions, as is well known in the art, judge whether to execute one of a first*

operation (an operation on the taken path) and a second operation (an operation on the fall through path)]; and

an interchanging unit operable *(Instruction Recombination Unit; Fig. 2, component 34)*, when only the first conditional instruction out of the first and second conditional instruction is decodable by a processor *(column 6, lines 17-24)*, to interchange

(a) the second conditional instruction with the first conditional instruction *(The instruction recombination unit interchanges the condition of a second conditional instruction (i.e. a conditional instruction in the source instruction set) with a condition of a first conditional instruction (i.e. a conditional instruction in the target instruction set) by interchanging a first and second conditional instructions in the instruction stream; column 6, lines 17-24)*, and

(b) an operation of the first operation with an operation of the second operation *(The instruction recombination unit interchanges an operation of the second operation (i.e. a conditional instruction in the source instruction set) with an operation of the first operation (i.e. a conditional instruction in the target instruction set) by interchanging a first and second operations in the instruction stream; column 6, lines 17-24)*.

Conclusion

21. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or

patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Benjamin P. Geib whose telephone number is (571) 272-8628. The examiner can normally be reached on Mon-Fri 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Huynh can be reached on (571) 272-4147. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Benjamin P Geib
Examiner
Art Unit 2181

2/6/06

HENRY W. H. TSAI
PRIMARY EXAMINER